Faculty Development Program
On
Cloud-enabled VLSI SoC design using open-source EDA tools

Under the banner of
Electronics and ICT academy, NIT Patna

06th - 10th May, 2020

Patrons

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Sponsored by

Meity and Govt. of India

Organized by

Department of Electronics and Comunication Engineering,
National Institute of Technology, Patna-800005

About NIT Patna

National Institute of Technology Patna is the 18th National Institute of Technology created by the Ministry of H.R.D. Government of India after rechristening the erstwhile Bihar College of Engineering Patna on 28.01.2004. NIT Patna marked its humble beginning in 1886 with the establishment of pleaders survey training school which was subsequently promoted to Bihar College of Engineering Patna in 1924. This made this institute the 6th oldest Engineering Institute of India. The Institute is situated on the south bank of holy river Ganges behind Gandhi Ghat (where the ash of father of the Nation, Mahatma Gandhi was offered in the river Ganges). The campus has a picturesque river view with historic building presenting a spectacle of architecture delight and natural beauty. The Institute imparts high level education training, research and development in science, engineering technology and humanities along with high quality education and values at UG, PG and Ph.D. level. At present the Institute offers courses in six major technical disciplines viz. Architecture, Civil Engineering, Computer Science & Engg., Electrical Engg., Electronics & Communication Engg. And Mechanical Engg. It also consists of well-established departments of Physics, Chemistry, Mathematics and Humanities and Social Sciences.

Electronics and ICT Academy

Ministry of Electronics and Information Technology, Government of India has instituted seven Electronics and Information & Communications Technology (ICT) Academies of which, the academy of NIT Patna is one. The Academy at NIT Patna aims to design and organize basic as well as specialized training programs in niche areas of electronics and ICT for the development of required knowledge base, skills and tools to equip the teaching community with better knowledge and understanding.

Overview

The semiconductor industry is undergoing a massive change with technologies like IOT, intelligent edge/cloud, mobility, automotive, 5G, AI, and ML, creating in major opportunities. The expectations of 50 billion connected devices by 2025 and the massive amounts of data that will need to be processed on edge analytics as well as on cloud will result in sharper insights for better decision-making applications and designing challenges. New, innovative approaches to SoC design will use non-Von Neumann architectural approaches with embedded neural networks to make problems like pattern recognition solvable in real time. Suddenly, the world of venture capital funded fabless semiconductor companies has exploded, as these companies propose innovative SoCs to solve “domain-specific” problems like vision-, sound-, or smell related pattern recognition. Being able to do a few specific types of operations extremely well now becomes much more important than doing a wide variety of things very well. Course like this will be a practical approach to VLSI System on Chip (SoC) Design provide guidance for aspiring designers and academicians who wish to join this parade of innovation. Here there is a potential that new ideas where the ability to translate algorithmic innovation to silicon can drive quantum steps forward in machine learning capability. This program would focus on the basic concept of SoC designing. Along with the theory session hands on session will also be conducted.

Objective and Scope

- Primary objective of this program is to provide an exposure of recent trends in SoC designing and their circuit applications.
- During this program our focus will be on developing the state-of-the-art in basic designing approaches, and practical designing challenges through interaction with industrial experts and some academicians from academic CFTI institutions such as IITs/NITs/IIITs including host institution.
- A comprehensive overview of the design criteria, methodology, skills, and knowledge needed for an SOC VLSI designer. It enables fresh engineering graduates to contribute in the industry from day one and create complex SOC designs
- This program can serve as an excellent platform to get the concepts of both basics and recent research advances in VLSI technology to the teaching and research community associated with the Departments of Electronics, Electrical and Computer Science etc.
- Finally, it will provide a unique opportunity to identify and to discuss potential collaborations among young researchers and faculty.

Course Content

- To study various components of RISC-V based SoC and review RISC-V picoSoC
- To understand importance of good vs bad floor plan and introduction to library.
- To design and characterize one library cell using open-source Layout tool and spice simulator
- To do pre-layout static timing analysis and understand the importance of good clock tree.
- To understand full-chip integration steps and implement E31 RISCV design using open-source

Outcomes

- By the end of the program, the participants should be able to understand the basics as well as recent research opportunities in SoC designing.
- They will be able to simulate the some basic designing, using cloud computing open source softwares.

Open-Source EDA Tools

- **Yosys – for Synthesis**
- **Graywolf – for Placement**
- **Qrouter – for Routing**
- **Netgen – for LVS**
- **Magic – for Layout and Floorplanning**
- **Qflow – RTL2GDS integration**
- **OpenSTA & Opentimer – Pre-layout and Post-layout Static timing analysis**

One-week FDP includes

- Virtual Coach platform with expert instructor guidance
- Cloud-based dedicated Virtual Machine to perform Design labs
- Intelligent Assessment Technology (IAT) and Project allocation
- 24 hours Lab access for 5 days and Instructor assistance on demand.
- Run EDA scripts, evaluate VLSI layout and Timing analysis reports on platform.

Who Can Participate

Faculty members of UGC/AICTE recognized Universities and Engineering colleges all over India, Research scholars (PhD only), students and Industry personals, however priority will be given to the faculty members.

Registration Fee

- **Faculty Member/Research Scholar: Rs 1500/-**
- **Ph.D/PG Students/B.Tech : Rs 1500/-**
- **Industry Personnel: Rs 2000/-**

Certificate will be given by Electronics & ICT Academy, NIT Patna.

Registration Process

1. Registration fee will be paid though online mode, the account details for this purpose is

   Account Name: NIT Patna
   Account No.: 50380476798
   IFSC Code: ALLA0212286

2. Link for registration: https://forms.gle/HVi5eQE9gnWKmctR7

3. The brochure of the program may be downloaded from the Institute website www.nitp.ac.in.

4. **Last date of registration: 04.05.2020**

Total -100 seats and the selection will be done on first-cum-first-serve basis. PDF file of online filled registration form with proof of registration fee paid will be send though email to **Dr. Sangeeta Singh. (email: sangeeta.singh@nitp.ac.in)**

FDP On

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(06th - 10th May, 2020)

REGISTRATION FORM

1. Name (block letter): ……
2. Gender: ……
3. Caste:……
4. DOB:……
5. Designation ……
6. Organization: ……
7. Address for communication: ……

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   Pin code: …… Ph. No.: ……

   E-mail: ……
8. Highest Academic Qualification: ……
9. Specialization: ……
10. Experience (in years):

    (a) Teaching: …… (b) Industrial: ……
11. Aadhar No:……

DECLARATION

I do hereby agree to abide by the rules and regulations of the FDP.

Place: ……

Date:……..……..

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Signature of the Applicant