# NATIONAL INSTITUTE OF TECHNOLOGY PATNA
# BIHAR – 800005

Deity, HRD Division, Ministry of ICT, Govt. of India Sponsored
Faculty Development Programme (FDP) on

## ANALOG ELECTRONIC CIRCUITS
## (Module: 01)

19th – 28th February, 2016

**Organized by Electronics and ICT Acadamey & Department of Electronics and Communication Engineering**

### Goal of Electronics and ICT Academy:

The main goal of the academy is to train the faculty members of different technological and other Institutes in different areas of Electronics and Information & Communications Technology of Bihar, Odisha, West Bengal, and Jharkhand. The resource persons will be from IITs/NITs. The courses would be conducted in the premises of NIT, Patna as well as at identified venues in these states for which all the resource persons and facilities will be provided by the Academy at NIT, Patna.

**States being catered to:** Bihar, Jharkhand, Odisha and West Bengal.

**About the Course:** Analog Electronic Circuits is one of the most fundamental and vital course for Electronic Engineers. This gives the very foundation for the Analog Design. Through this course candidate can have the basic introduction for VLSI. After attending the course candidate will get exposure of different State-of-art methods for the analysis of Analog circuits.

### Course Contents:

**BJT Amplifier Circuits:** BJT Characteristics, Biasing, Linear Models, Single Stage Amplifiers: CE, CC and CB Amplifiers, Parasitic Capacitances, Hybrid-pi model, Frequency Response of BJT Amplifiers.
**MOSFET Amplifier Circuits:** MOSFET Characteristics, Biasing, Linear Models, Single Stage Amplifiers: CS, Source Follower, Common-Gate Configurations, Parasitic Capacitances, Frequency Response of MOS Amplifiers,
**Feedback Amplifiers:** Types of Feedback Configurations and their Analysis, BJT Amplifiers with Feedback, MOSFET amplifiers with Feedback
**BJT and MOS Current Mirrors:** Simple Current Mirror (CM), Base Current Compensated CM, Wilson CM, Cascode CM, Modified Wilson CM, MOS CMs: Simple CM, Wilson CM, Cascode CM and Modified Wilson CM.
**BJT and MOSFET Sinusoidal Oscillators:** Amplifiers with Positive Feedback, Barkhausen Criterion, Classical Oscillators using BJT and MOS Amplifiers, RC Phase Shift, Wien Bridge, Hartley, Colpitts and Others,.
**Differential Amplifiers:** Emitter Coupled Differential Pair, Linear Range of Operation, Extending Liner Range with Emitter Degeneration, Active Load, Current Source Biasing, Determination of Ad, Ac, CMRR, Rid and Rout, Source Coupled Differential Amplifier: Analysis, Differential Amplifier with active load and current source biasing.
**Bipolar OP-AMPS:** Input stages, Intermediate Gain Stages, Output Stages, Architecture of µA 741 type op-amp, DC analysis and small signal analysis, Gain Bandwidth Product, Large Signal Behaviour and origin of slew rate, Non-ideal parameters, Input Bias Current, Offset Voltage, CMRR, PSRR etc.
**MOS OP-AMPS:** Various MOS op-amp architectures, Analysis of typical CMOS op-amp architectures

### Expert Speakers:

**Prof. S. C. Dutta Roy, Formerly at IIT Delhi**

**Prof. Raj Senani, NSIT, New Delhi**

**Prof. G. S. Visweswaran, Formerly at IIT Delhi**

**Prof. K. Radhakrishna Rao, Formerly at IIT Madras**

**Prof. Shanthi Pawan, IIT Madras**

**Prof. K. V. V. Murthy, Formerly at IIT Bombay**

**Dr. Aniruddhan Sankaran, IIT Madras**

**Dr. Nagendra Krishnapura, IIT Madras**

**Prof. P V A Ananda Mohan, formerly at ITI**

**Dr. Shouri Chatterjee, IIT Delhi**

**Prof. M. Tripathi, NIT Patna**

**Eligibility:** The programme is open to faculty from Electronics Engineering, Electronics and Communication Engineering, Electrical and Electronics Engineering and other allied disciplines from Engineering Colleges in Bihar, Jharkhand, Odisha and West Bengal. Participants from

### Registration Fee:

For Faculty: Rs. 3000 /-

**How to Apply:**
A filled in form which can be downloaded from the website www.nitp.ac.in in the prescribed format duly signed and sponsored by appropriate authorities along with the demand draft has to be sent to the coordinator by post. It is also mandatory to send scanned application form and DD through mail to munish@nitp.ac.in.
The DD must be drawn in favour of "**Director, NIT Patna**" payable at Patna.

Registration fee can also be deposited through NEFT and the hard copy of bank transaction has to be attached with the application. The bank details are as follows:
**Bank Name: Allahabad Bank, NIT Patna**
**A/c No: 20353663911**
**IFSC Code: ALLA0212286**
**A/c Holder Name: Registrar, NIT Patna**

**Selection Criterion:** Selection will be done on first-cum-first-serve basis and the confirmed candidates will be notified immediately. The maximum numbers of participants will be 50 (fifty).

**Last date of submission of application: 12.02.2016**

**FORMAT OF APPLICATION**

**Electronics and ICT Academy**

**Faculty Development Programme**

**On**

**ANALOG ELECTRONIC CIRCUITS (MODULE: 01)**

**(19th - 28th February 2016)**

1. **NAME:**
2. **DESIGNATION:**
3. **INSTITUTION:**
4. **E-MAIL:**
5. **DD No.:** **Amount Rs. 3000/-**
   **BANK NAME:**

   **DATE:**
6. **ADDRESS FOR CORRESPONDENCE:**
7. **EDUCATIONAL QUALIFICATIONS WITH SPECIALIZATION:**
8. **SUBJECTS TAUGHT SO FAR:**
9. **NO. OF REFRESHER COURSES / WORKSHOPS ATTENDED:**
10. **EXPERIENCE (IN YEARS)**
    **TEACHING:**

    **RESEARCH:**

    **INDUSTRY:**
11. **ACCOMODATION REQUIRED: YES / NO**
12. **DO YOU BELONG TO SC / ST: YES / NO**

**SPONSORSHIP CERTIFICATE**

Dr/Mr./Ms. ……. is an employee of our Institute / Organization and is hereby sponsored to participate in the FDP on Analog Electronic Circuits (Module 01) sponsored by ICT Academy at NIT Patna during 19th February 2016 to 28th February 2016 at the National Institute of Technology (NIT), Patna.

Place:

Date:

**Signature of the Head of the Institution**

**(with official seal)**

**ADDRESS FOR CORRESPONDENCE**

**Prof. M. P. Tripathi,**
Professor Emeritus & Course Coordinator "AEC 2016"
Dept. of. Electronics and Communication Engineering,
National Institute of Technology, Patna,
Bihar – 800005.
Ph: 7549905629, 9560606324
Email: munish@nitp.ac.in

## Patron

**Prof. Asok De**

Director, NIT Patna

## Coordinator

**Prof. M. P. Tripathi**

Professor Emeritus,
Dept. of. E.C.E, NIT Patna

## Co-Cordinators

**Dr. Puli Kishore Kumar**

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**Dr. A. K. Bhandari**

Assistant Professor,
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## Advisory Committee

**Prof. D. K. Singh**

**Prof. U. S. Triar**

**Prof. J. Ghosh**

## Organizing Committee

**Prof. B. C. Sahana**

**Prof. G. Pradhan**

**Prof. Gaurav Kaushal**

**Prof. Wasim Akram**

**Dr. Asit Narayan**